

Amendments to the Claims

The listing of claims will replace all prior versions, and listings of claims in the application.

1. (Currently Amended) An integrated circuit (IC) output stage protection system, comprising:

a ~~relatively low voltage CMOS~~ first NMOS device, having a gate configured to be coupled to an output of an IC logic core and a source coupled to a current source;

a ~~first relatively high voltage CMOS~~ second NMOS device, having a source coupled to a drain of said ~~relatively low voltage CMOS~~ first NMOS device and a gate coupled to a biasing circuit that biases said ~~first relatively high voltage CMOS~~ second NMOS device so that said ~~relatively low voltage CMOS~~ first NMOS device operates in a saturation region; and

one or more diodes coupled between an output node and a gate of a ~~second relatively high voltage CMOS~~ third NMOS device, having a source coupled to a drain of said ~~first relatively high voltage CMOS~~ second NMOS device and a drain coupled to said output node, wherein said one or more diodes substantially protect said ~~CMOS~~ NMOS devices so that they operate within a device voltage rating;

wherein an operating voltage of said first NMOS device is lower than an operating voltage of said second NMOS device, and wherein said operating voltage of said first NMOS device is lower than an operating voltage of said third NMOS device;

2. (Currently Amended) The IC output stage protection system of claim 1, wherein said one or more diodes are coupled to said gate of said ~~second relatively high voltage CMOS~~ third NMOS device through a resistor.

3. (Currently Amended) The IC output stage protection system of claim 1, wherein at least one of said one or more diodes comprises a ~~CMOS~~ an NMOS device configured as a diode, said ~~CMOS~~ NMOS device having a guard ring coupled to first and second contacts on a P-substrate.

4. (Original) The IC output stage protection system of claim 1, further comprising:

an input/output (I/O) pad electrostatic discharge (ESD) protection circuit coupled to said output node.

5. (Currently Amended) The IC output stage protection system of claim 4, wherein said I/O pad ESD protection circuit comprises:

a first set of one or more diodes coupled between an I/O pad and a local net;

a second set of one or more diodes coupled between a ground and said I/O pad;

a ~~CMOS~~ an NMOS device having a drain coupled to said local net, a source coupled to said ground, and a gate coupled to an output of an inverter;

a first resistor coupled between said local net and an input of said inverter;

a capacitor coupled between said input of said inverter and said ground; and

a second resistor coupled between said local net and said ground.

6. (Currently Amended) An integrated circuit (IC) output stage protection system, comprising:

a first pair of ~~relatively low voltage CMOS~~ NMOS devices, each having a gate configured to be coupled to respective IC logic core outputs and a source coupled to a current source;

a ~~first~~ second pair of ~~relatively high voltage CMOS~~ NMOS devices, each having a source coupled to a respective drain of said first pair of ~~relatively low voltage CMOS~~ NMOS devices and a gate coupled to a biasing circuit that biases said second ~~first~~ pair so that said first pair of ~~relatively low voltage CMOS~~ NMOS devices operate in a saturation region;

a ~~third~~ second pair of ~~relatively high voltage CMOS~~ NMOS devices, each having a source coupled to a respective drain of said second ~~first~~ pair of ~~relatively high voltage CMOS~~ NMOS devices and a drain coupled to first and second output nodes, respectively;

wherein an operating voltage of said first pair of NMOS devices is lower than an operating voltage of said second pair of NMOS devices and said operating voltage of said first pair of NMOS devices is lower than an operating voltage of said third pair of NMOS devices;

a first set of one or more diodes coupled between said first output node and respective gates of said ~~second~~ third pair of ~~relatively high voltage CMOS~~ NMOS devices; and

a second set of one or more diodes coupled between said second output node and said respective gates of said ~~second~~ third pair of ~~relatively high voltage~~ CMOS NMOS devices;

wherein said first and second sets of one or more diodes substantially protect said CMOS NMOS devices so that they operate within a device voltage rating.

7. (Currently Amended) The IC output stage protection system of claim 6, wherein said first and second sets of one or more diodes are coupled to said respective gates of said ~~second~~ third pair of ~~relatively high voltage~~ CMOS NMOS devices through a resistor.

8. (Currently Amended) The IC output stage protection system of claim 6, wherein:

said first pair of ~~relatively low voltage~~ CMOS NMOS devices comprises a pair of relatively thin oxide devices; and

said ~~first and second~~ and third pairs of ~~relatively high voltage~~ CMOS NMOS devices comprise a first and second pair of relatively thick oxide devices.

9. (Original) The IC output stage protection system of claim 6, wherein said first and second sets of one or more diodes each comprise two diodes.

10. (Currently Amended) The IC output stage protection system of claim 6, wherein at least one of said diodes comprises a CMOS an NMOS device configured as a diode, said CMOS NMOS device having a guard ring coupled to first and second contacts on a P-substrate.

11. (Original) The IC output stage protection system of claim 6, further comprising:

a first input/output (I/O) pad electrostatic discharge (ESD) protection circuit coupled to said first output node; and

a second I/O pad ESD protection circuit coupled to said second output node.

12. (Currently Amended) The IC output stage protection system of claim 11, wherein said first and second I/O pad ESD protection circuits each comprise:

a first set of one or more diodes coupled between an I/O pad and a local net;

a second set of one or more diodes coupled between a ground and said I/O pad;

~~a CMOS~~ an NMOS device having a drain coupled to said local net, a source coupled to said ground, and a gate coupled to an output of an inverter;

a first resistor coupled between said local net and an input of said inverter;

a capacitor coupled between said input of said inverter and said ground; and

a second resistor coupled between said local net and said ground.

13. (Currently Amended) An integrated circuit (IC) output stage protection system, comprising:

first and second input/output (I/O) pad electrostatic discharge (ESD) protection circuits coupled to respective first and second output nodes; and

an output stage, including:

~~first and second relatively low voltage CMOS devices~~ first and second NMOS devices having respective gates configured to be coupled to first and second IC core outputs, respectively, and respective sources coupled to a current source,

~~first and second relatively high voltage CMOS devices~~ third and fourth NMOS devices having respective sources coupled to respective drains of said first and second ~~relatively low voltage CMOS~~ NMOS devices and respective gates coupled to a biasing circuit,

~~third and fourth relatively high voltage CMOS~~ fifth and sixth NMOS devices having respective sources coupled to respective drains of said ~~first and second relatively high voltage CMOS~~ third and fourth NMOS devices and respective drains coupled to first and second output nodes, respectively,

wherein an operating voltage of said first and second CMOS devices is lower than an operating voltage of said third and fourth NMOS devices and said operating voltage of said first and second NMOS devices is lower than an operating voltage of said fifth and sixth NMOS devices;

a first set of one or more diodes coupled between said first output node and respective gates of said ~~third and fourth relatively high voltage CMOS~~ fifth and sixth NMOS devices, and

a second set of one or more diodes coupled between said second output node and said respective gates of said ~~third and fourth relatively high voltage CMOS~~ fifth and sixth NMOS devices;

wherein said output stage protection system substantially protects said ~~CMOS~~ NMOS devices so that they operate within a device voltage rating during IC power up/power down and ESD events.

14. (Currently Amended) The IC output stage protection system of claim 13, wherein said first and second sets of one or more diodes are coupled to said respective gates of said ~~third and fourth relatively high voltage CMOS~~ fifth and sixth NMOS devices through a resistor.

15. (Original) The IC output stage protection system of claim 13, wherein said first and second sets of one or more diodes each comprise two diodes.

16. (Currently Amended) The IC output stage protection system of claim 13, wherein at least one of said diodes comprises a ~~CMOS~~ an NMOS device configured as a diode, said ~~CMOS~~ NMOS device having a guard ring coupled to first and second contacts on a P-substrate.

17. (Currently Amended) The IC output stage protection system of claim 13, wherein said first and second ~~relatively low voltage CMOS~~ NMOS devices each comprise a 1.2 V device; and
said ~~first, second, third, and fourth relatively high voltage CMOS~~ third, fourth, fifth, and sixth NMOS devices each comprise a 2.5 V device.

18. (Currently Amended) The IC output stage protection system of claim 17, wherein a voltage difference between any two terminals of said first and second ~~relatively low voltage CMOS~~ NMOS devices does not exceed approximately 1.32 V, and wherein a voltage difference between any two terminals of ~~first, second, third, and fourth~~

~~relatively high voltage CMOS~~ third, fourth, fifth, and sixth NMOS devices does not exceed approximately 2.75 V.

19. (Currently Amended) The IC output stage protection system of claim 17, wherein said biasing circuit biases said gates of said ~~first and second relatively high voltage CMOS~~ third and fourth NMOS devices so a drain voltage of said first and second ~~relatively low voltage CMOS~~ NMOS devices does not exceed approximately 1.2 V.

20. (Currently Amended) The IC output stage protection system of claim 13, wherein said first and second I/O pad ESD protection circuits each comprise:

- a first set of one or more diodes coupled between an I/O pad and a local net;
- a second set of one or more diodes coupled between a ground and said I/O pad;
- ~~a CMOS~~ an NMOS device having a drain coupled to said local net, a source coupled to said ground, and a gate coupled to an output of an inverter;
- a first resistor coupled between said local net and an input of said inverter;
- a capacitor coupled between said input of said inverter and said ground; and
- a second resistor coupled between said local net and said ground